Jameco Part number 126703

VECTOR 2X

COMPASS

MODULE

Application Notes

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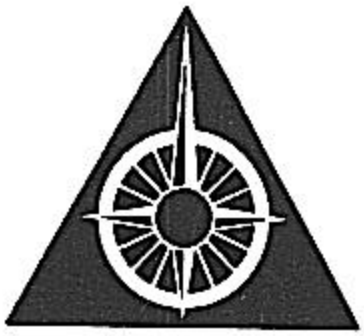
January 1996



PRECISION NAVIGATION, INC.

Jameco Part number 126703

Vector 2X Application Notes

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1.0 DESCRIPTION

Precision Navigation, Inc.'s Vector 2X is a low-cost, 2-axis compass module suitable for OEM applications. Using PNI's patented magneto-inductive magnetometer technology (United States Patent #4,851,775), the Vector 2X delivers high accuracy, low power, and low cost in the same small size package. The module delivers 2-degree accuracy with 1-degree resolution, outperforming all compasses in its price range. The Vector 2X is simple to calibrate and incorporate into systems designed by first-time users or experienced experts.

The Vector 2X Compass Module offers:

- 2° accuracy, 1° resolution
- Small size and weight: 1.50" x 1.30" x 0.39"; 0.3 oz.
- Low power requirement: single-sided 5 volt (regulated) supply, less than 10 milliamp (mA) draw (<1 mA in powerdown mode)
- Low resolution output is 5 hertz (Hz); high resolution output is 2.5 Hz
- Input voltage on all I/O ports: -0.3 to V_{DD} +0.3 volts
- Output voltage on all I/O ports: -0.3 to V_{DD} +0.3 volts
- Output ports can source or sink 5 mA
- 3-wire serial output format (Motorola SPI- and National Microwire-compatible) makes for easy installation into OEM systems
- Hard iron calibration
- Raw uncalibrated output option
- Pin-selectable Binary-Coded Decimal (BCD) or Binary output format
- Polled or continuous mode options
- Master or slave capability for data clock generation
- Operating temperature range: -20°C to 70°C

Possible applications for the Vector 2X include:

- GPS system backup azimuth data
- Remote terrestrial antenna direction indicators
- Auto and industrial navigation systems
- Consumer and hobbyist markets
- Survey instruments
- Laboratory equipment
- Robotics systems
- Azimuth indicators

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Vector 2X Application Notes

2.0 OVERVIEW

2.1 Features and Specifications

A general board layout of the Vector 2X is shown in Figure 1; Table 1 presents the pin configuration. The pin programmability allows users to set up the compass for their specific needs. The Vector 2X uses a synchronous serial port for communication to the host device (compatible with Motorola SPI, QSPI, and National Microwire). The output data format is pin-selectable between BCD and binary mode, and the serial data output (SDO) is tri-stated when the unit is not selected in Slave mode.

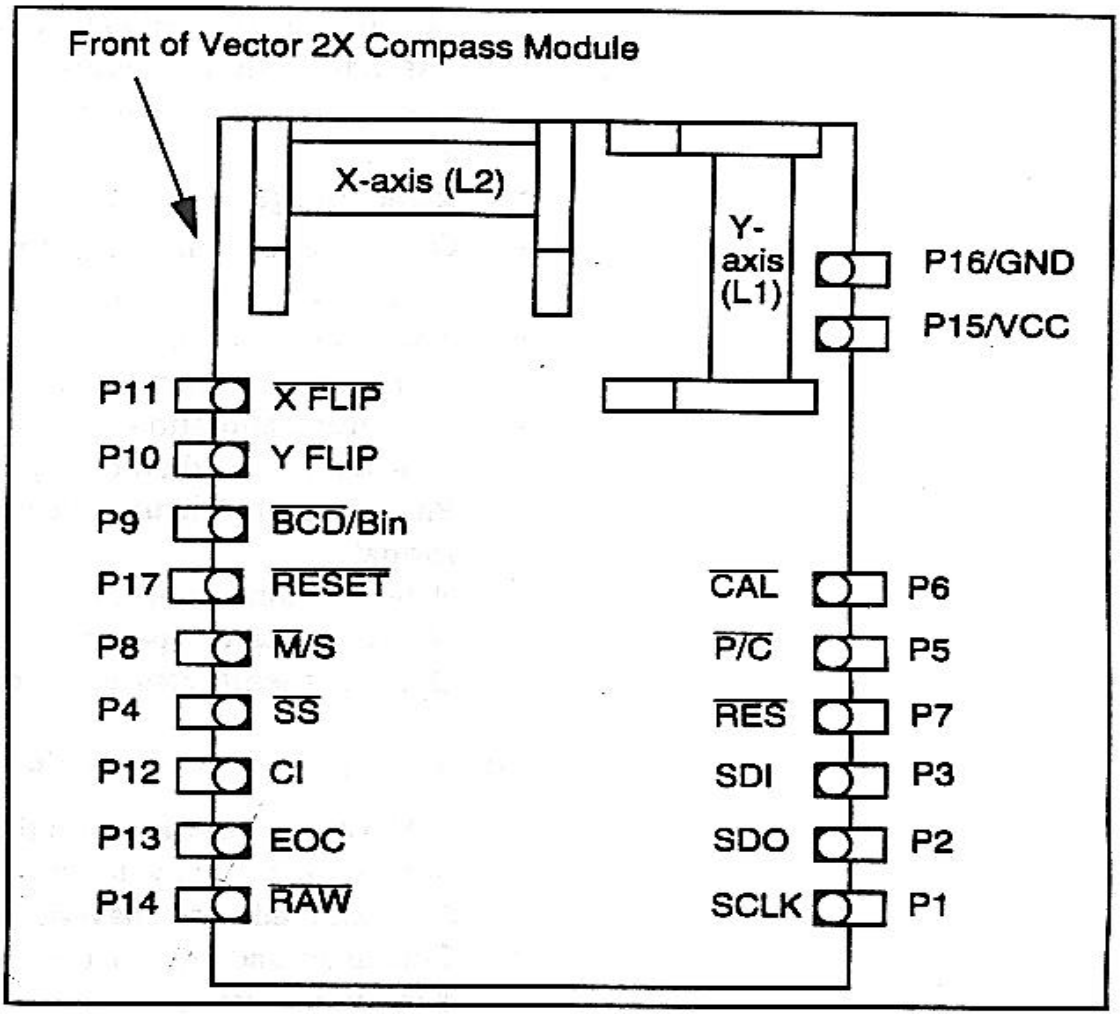

Figure 1: Vector 2X Board Layout

Table 1: Vector 2X FUNCTION DESCRIPTION

Pin	Name	Description	Input or Output
P1	SCLK	Serial Clock Input; Data valid on rising clock edge%r*%r	Input/Output
P2	SDO	Serial Data Output	Output
P3	SDI	Serial Data Input	No Connect
P4	$\overline{SS}$	Slave Select; Active Low	Input
P5	$\overline{P/C}$	Poll / Continuous; Active when P/C = Low	Input
P6	$\overline{CAL}$	Calibrate Select; Active when CAL = Low	Input
P7	$\overline{RES}$	Resolution; Low Resolution when RES = Low	Input
P8	$\overline{M/S}$	Master/Slave select; Master Mode when M/S = Low	Input
P9	BCD/Bin	BCD/Binary select; BCD when BCD/Bin = Low	Input
P10	$\overline{Y\ FLIP}$	Flip Y-axis direction. Low = Normal Direction	Input
P11	X FLIP	Flip X-axis direction. High = Normal Direction	Input
P12	CI	Calibrate indicator signal; Active High	Output
P13	$\overline{EOC}$	End of Conversion signal; Conversion complete on rising edge of EOC	Output
P14	RAW	Raw data mode select pin; Active Low	Input
P15	VCC	5 volt power input	
P16	GND	Power supply return	
P17	RESET	Reset pin; Active Low	Input

* Maximum clock rate is 1 MHz in Slave mode

The $\overline{\text{X FLIP}}$ and $\overline{\text{Y FLIP}}$ pins provide a means to re-orient the Vector 2X so that it can be mounted in an inverted position. The $\overline{\text{X FLIP}}$ pin inverts the north and south directions, and the Y FLIP inverts the east and west directions. The normal mode is $\overline{\text{X FLIP}}$ = 1 and Y FLIP = 0.

The $\overline{\text{RES}}$ pin is normally grounded unless higher resolution output is required for more counts in the RAW mode or for areas with weak magnetic field strength (with the Vector 2X in either Master or Slave mode). High resolution output is 2.5 Hz; low resolution output is 5 Hz.

The $\overline{\text{P/C}}$, $\overline{\text{CAL}}$, $\overline{\text{RESET}}$ and SS pins must be logic high during powerup; these four ports have internal 100 kohm pullup resistors and must be connected to bidirectional I/Os set to inputs. Otherwise, the Vector 2X will hang upon powerup and can be reset by toggling the $\overline{\text{RESET}}$ pin after startup.

The Vector 2X is in sleep mode under normal operation and draws very low current, only becoming active when acquiring or outputting data. The power required in sleep mode is less than 1 mA; during operation the power required rises to less than 10 mA.

2.2 Operating modes of the Vector 2X

The Vector 2X operates in three modes: Master mode, Slave mode, and RAW mode. The configurations for running the Vector 2X in each of these modes are described below:

2.2.1 Master mode

The Vector 2X can run in Master mode and generate the serial data clock. In Master mode the Vector 2X clocks out the data using an internally-generated clock. This feature allows the Vector 2X to load data into devices such as serial-to-parallel shift registers without the intervention of a host processor. When in Master mode the EOC provides a positive edge to indicate the complete 16-bit word has been sent. SDO is never tri-stated in Master mode.

Figure 2 shows the timing diagram for the Vector 2X in Master mode. The $\overline{\text{M/S}}$ pin must be tied low to enable Master mode, and SS should not be connected. The $\overline{\text{P/C}}$ pin is used to request data from the Vector 2X, and EOC is used to frame data. The Vector 2X, in Master mode, can collect and output heading information in either polled or continuous mode. Pulsing the $\overline{\text{P/C}}$ pin low for a minimum of 10 millisecond (msec) polls the compass for a single reading, and holding the $\overline{\text{P/C}}$ pin low causes the Vector 2X to output continuously (both $\overline{\text{P/C}}$ modes are represented in Figure 2 - and subsequent figures - by a solid line showing the pulsed polled mode, and a dotted line illustrating the continuous mode). EOC

frames the continuous readings; the readings are updated at a rate of approximately 5 Hz at low resolution and 2.5 Hz at high resolution. The SCLK pin is an output in Master mode; the SCLK pin outputs 16 clock pulses at a rate of 4 KHz for each conversion. If P/C is held low, the Vector 2X starts another cycle of readings automatically. The first six bits output from the SDO pin will always be zero in either Binary or BCD mode, and the first significant bit (FSB) after the first six bits will always be a zero in Binary mode.

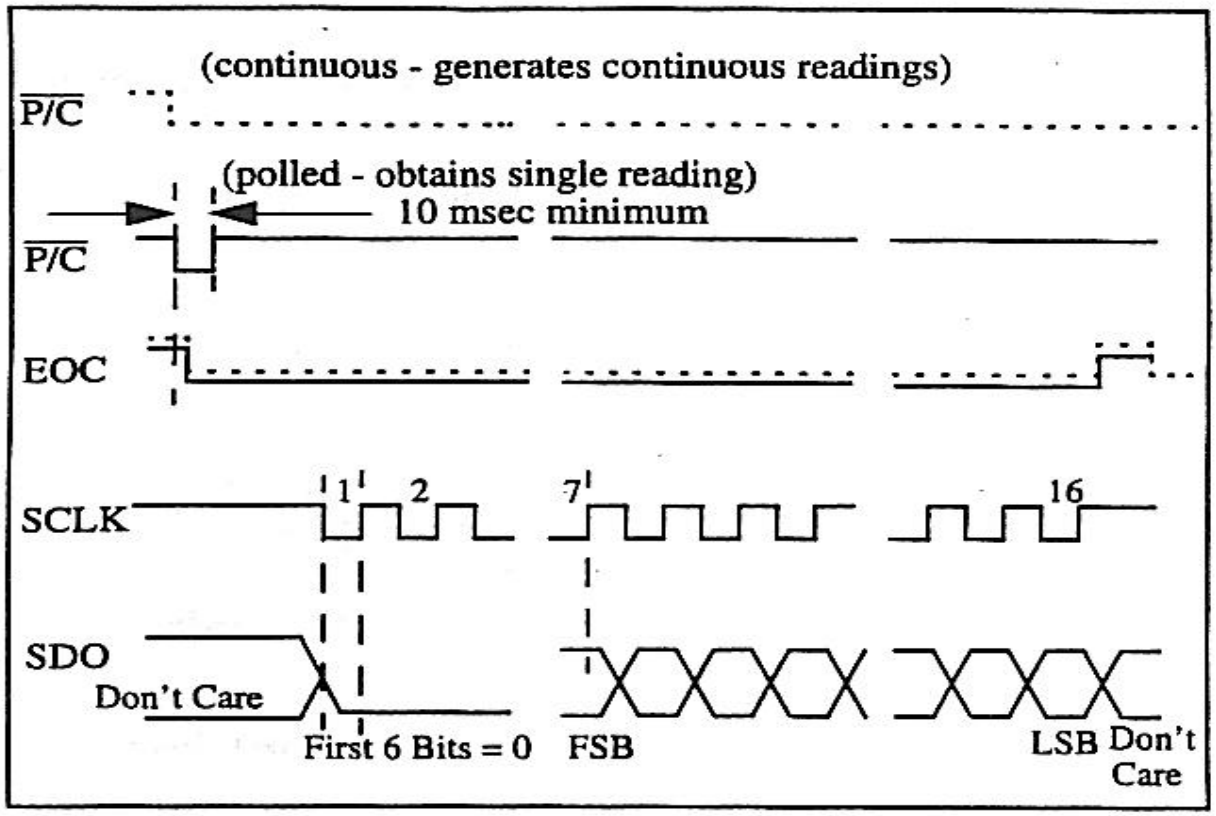

Figure 2: Data Clock Timing Diagram
(Master Mode 16-bit Data Format)

2.2.2 Slave Mode

When the Vector 2X operates in Slave mode, the host generates the data clock; the M/S pin must be open or tied high to enable this mode. The Vector 2X, in Slave mode, can be connected to a synchronous serial port along with other devices. SDO remains in a tri-state mode until the host requests data from the device by toggling and holding SS low for the duration of the read, at which time it becomes an output. The EOC pin supplies a rising edge to indicate that the Vector 2X has completed the calculations. This feature frees the serial port for other devices to communicate with the host.

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Figure 3 illustrates the data clock timing diagram with the Vector 2X in Slave mode, 16-bit data format. In Slave mode, the SCLK is an input. External SCLK must be supplied by the host processor to clock out data on SDO; frequencies of up to a maximum of 1 MHz are acceptable. Sixteen complete clocks (i.e., 16 falling edges **and** 16 rising edges) must be supplied to the Vector 2X in order to obtain data; otherwise, data may remain in the Vector 2X registers and the compass will hang. When the P/C pin is held low in Slave mode, the Vector 2X outputs a single heading until polled again; minimum pulse width on P/C is 10 msec. The timing between the rise of EOC and the falling edge of SS should be greater than 10 msec; data from the Vector 2X is output on the falling edge of SCLK and valid on the rising edge of each SCLK pulse. The first six leading 0s in the data format are constant in both Binary and BCD formats. The FSB will always be a zero in binary mode. The host must clock out all 16 bits from the Vector 2X to complete data transfer before attempting to acquire new data.

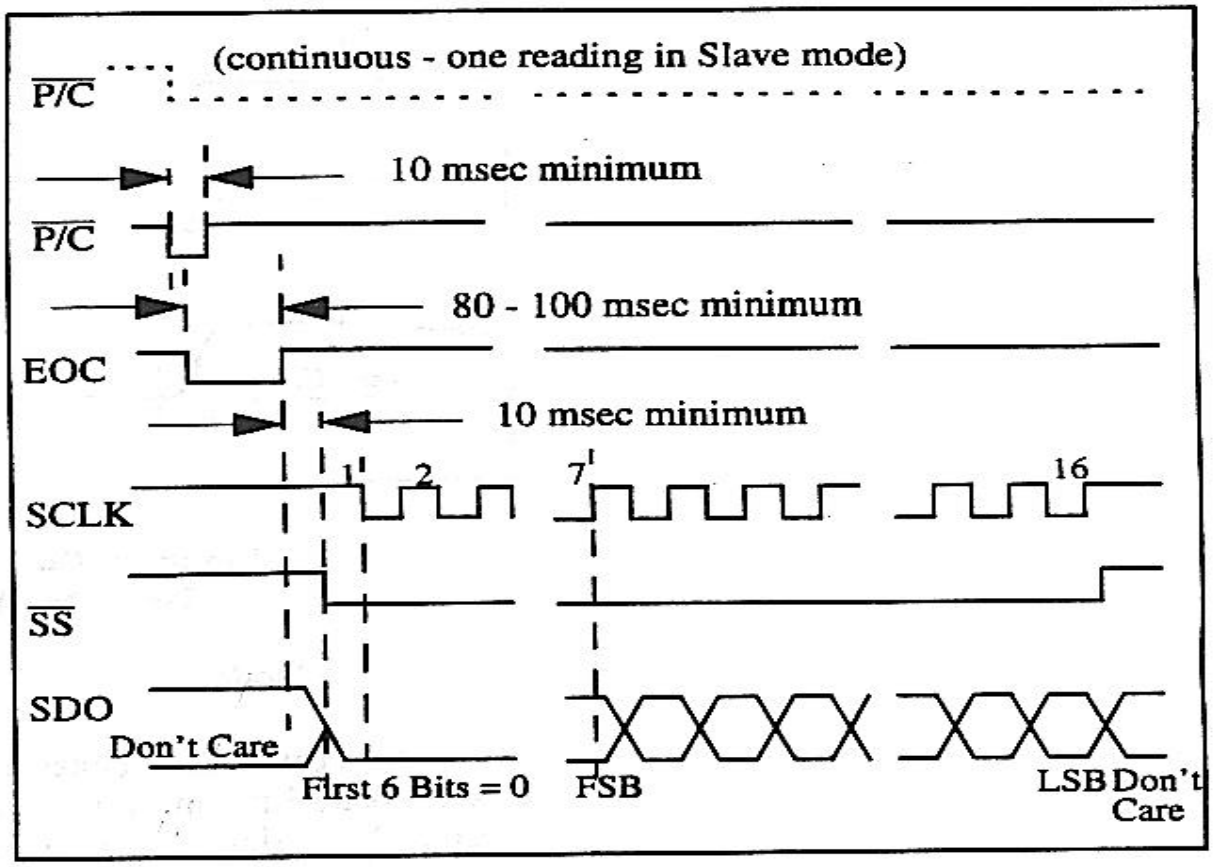

Figure 3: Data Clock Timing Diagram
(Slave Mode 16-bit Data Format)

2.2.3 RAW Mode

RAW data output is only available in Slave mode and not in Master mode. The SCLK pin is an input in RAW mode. Figure 4 displays the RAW mode data format. The M/S pin must be open or tied high to enable this mode, and the RAW pin must be tied low. The data format is available only in Binary output format, as four bytes (total 32 bits). The outputs are signed 16-bit integers; the first two bytes make up the binary number of the X-axis field intensity, and the last two bytes are the binary number for the Y-axis field intensity. The 16-bit values for the X-axis and Y-axis are not calibrated for magnetic scale.

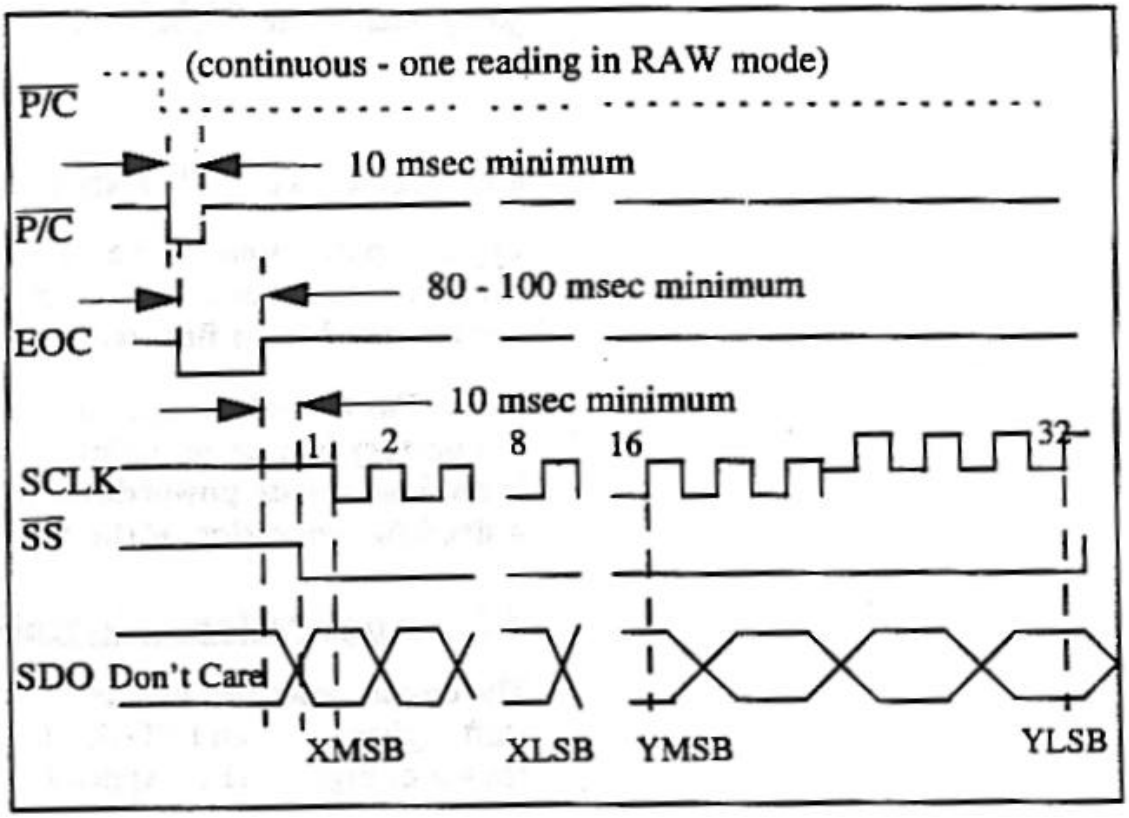

Figure 4: Raw Data Mode Format
(Slave Mode only, 16-bit Data Format)

3.0 CALIBRATION AND RESET

3.1 Calibrating the Vector 2X

Hard iron distortions from magnetized materials can cause the compass to display improper heading and RAW mode information. The CAL pin is used to calibrate offsets caused by these hard iron distortions. The Vector 2X measures the magnetic field strength in both the X-axis and Y-axis; calibration removes the distortion, and proper heading is obtained.

To calibrate the unit, pulse the $\overline{\text{CAL}}$ pin low for at least 10 msec, then rotate the Vector 2X in a half-circle (180 degrees). Pulse the CAL pin again for at least 10 msec and calibration is complete. When CAL is pulsed the first time, the CI pin goes high and stays high until the CAL pin is pulsed a second time. To abort the calibration or clear a previous calibration, pulse the CAL pin twice without moving the Vector 2X.
Note: $\overline{\text{P/C}}$ cannot be low when the Vector 2X is in calibration mode.

3.2 Resetting the Vector 2X

In the event the Vector 2X enters an unknown state or hangs, it may be necessary to reset the processor. Reset is performed by applying a low-going pulse to the $\overline{\text{RESET}}$ pin for a duration of not less than 10 msec.

4.0 APPLICATIONS FOR THE VECTOR 2X

Typical applications for the Vector 2X are described below; they demonstrate how to connect the Vector 2X to various types of circuits and **are not intended to be finished designs.**

Note: For the schematics shown in Figures A1 to A3 of Appendix A, the battery is used to maintain RAM data, so hard iron calibration is not lost during powerdown of circuit. Regulated +5 volt is still required for operation of the Vector 2X.

4.1 Application 1: Serial-to-Parallel Conversion

The circuit described here is a simple Vector 2X with serial-to-parallel shift registers and an LED display. The schematic for this application is shown as Figure A1 in Appendix A.

The Vector 2X is used in the following configuration:

Inputs:	$\overline{\text{M/S}}$ = 0	Master mode operation
	$\overline{\text{BCD}}$/Bin = 0	BCD output format
	$\overline{\text{RES}}$ = 0	Low resolution
	X FLIP = open	X normal
	$\overline{\text{Y FLIP}}$ = 0	Y normal
	$\overline{\text{RAW}}$ = open	Not RAW magnetometer output mode; inaccessible in Master mode

Figure 5 illustrates the timing diagram for this arrangement.

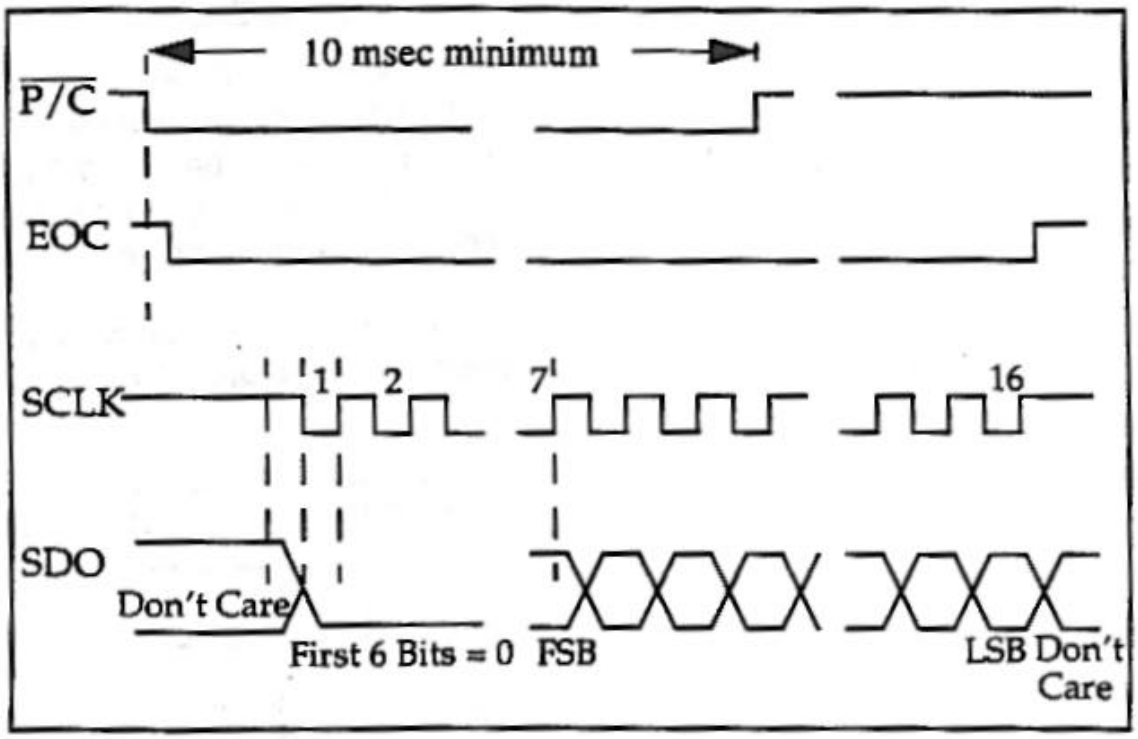

Figure 5: Timing Diagram for Connecting Vector 2X with Serial-to-Parallel Shift Registers

In this configuration, the Vector 2X is ready to output data to the shift registers when the P/C pin is grounded. If P/C is held low continuously, the heading data should be read out entirely before the Vector 2X outputs the next reading. SDO of the Vector 2X is connected to the serial input of the shift registers, which converts the serial data stream to a parallel format. The data from the Vector 2X is clocked with the SCLK signal, and the format is most significant bit (MSB) first. Ten bits are required to indicate 0 to 359 degrees (BCD), and the first six bits are always sent as zeroes. The parallel outputs of the shift registers are connected to two 8-bit latches. The data is latched on the rising edge of EOC; this EOC output frames the data and drops low at the beginning of the transfer and returns high after the last bit is transferred. When P/C=0, the Vector 2X acquires heading information and outputs the data when the calculations are complete. The data at the output of the latches is BCD-formatted data which can be connected to an LCD or LED through the appropriate display driver ICs. The Vector 2X acquires and outputs heading data for as long as the P/C pin is pulled low; when the P/C pin is pulled high, the Vector 2X finishes the last heading, outputs the data and then returns to sleep mode.

4.2 Application 2; Vector 2X Connected to a Motorola Processor

The Vector 2X can be connected to a Motorola 68HC705C8 processor, or similar processor, with a synchronous serial bus. A good discussion on SPI can be found in any Motorola Microprocessor, Microcontroller and Peripheral Data handbook. Sample SPI read code can be found in Appendix B; its corresponding schematic is shown in Figure B1.

Figure 6 shows the timing diagram for this connection; the schematic is presented in Figure A2 of Appendix A.

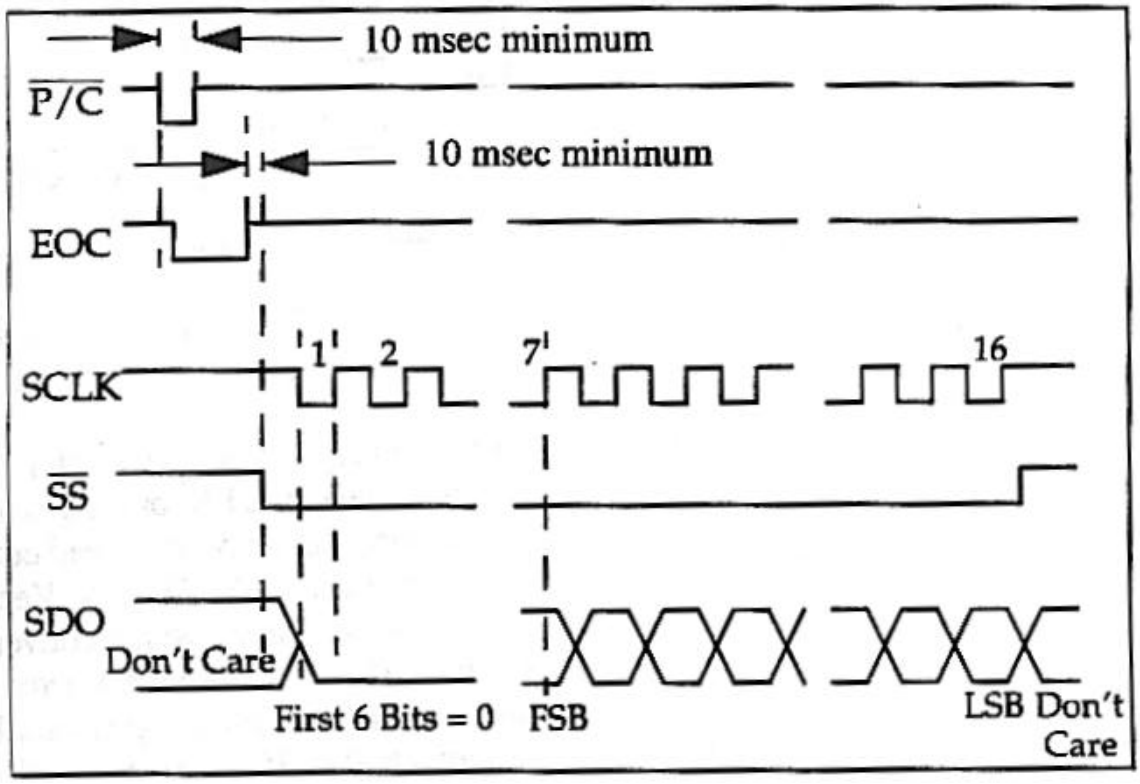

Figure 6: Timing Diagram for Connecting Vector 2X to a Motorola or Intel-Type Processor

As shown in Figure A2, the Vector 2X shares the serial bus with a MC14489P display driver. The SCLK line from the processor is connected to both the display driver and the Vector 2X; SDO is connected to PD2/MISO (master in, slave out) and SDI is not connected. The processor requests heading data from the Vector 2X, retrieves the data, reformats the data into BCD format suitable for the display driver, then outputs the data to the display driver. (The output from the Vector 2X in this case is set to Binary output mode, but it can also be set to BCD format if so desired.)

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Appendix A

Schematics for Section 4.0

4.3 Application 3; Vector 2X Connected to an Inteltype Processor

Some applications may employ the Vector 2X to control a stepper motor to keep the orientation of the directional component of the system constant with the direction of the compass. In this configuration, the Vector 2X is connected to a non-SPI processor (see Figure A3 of Appendix A). To start the Vector 2X, the host drops P/C for 10 msec and raises it again, which initiates the compass data acquisition process. The EOC line drops soon after the falling edge of P/C and returns to a high state when the heading calculation is complete; at this time, the data is ready and can be retrieved from the Vector 2X by dropping SS and providing 16 complete clocks to SCLK.

The data is valid on each rising edge of the 16 clock pulses of SCLK. The processor must supply the SCLK pin with the serial data clock; 16 complete clocks are required to transfer all of the data from the Vector 2X (see Figure 6 for timing diagram). The data from the Vector 2X appears at SDO and must be logically ORed with the accumulator, then shifted right eight times for each byte.

An alternate method for connecting the Vector 2X to a host processor is illustrated in Figure A4 of Appendix A; this configuration can be used if there are no other serial devices to be connected.

The P/C pin and the SS pin are connected together to reduce the number of I/O pins required. The EOC pin can be connected to the processor to signal the processor that the data is ready to be clocked out using SCLK. This application ties up the serial port for the entire time the Vector 2X is calculating the heading. The P/C pin is kept low until the data is retrieved only because it is tied together to the SS pin; P/C does not **have** to be held low. Toggling P/C before the data is completely output causes the Vector 2X to overwrite the old data, even if there is untransmitted data from the previous conversion.

Note: The P/C, CAL, RESET and SS pins must be logic high during powerup; these ports have internal 100 kohm pullup resistors and must be connected to bidirectional I/Os set to inputs. Otherwise, the Vector 2X will hang and can be reset by toggling the RESET pin after startup.

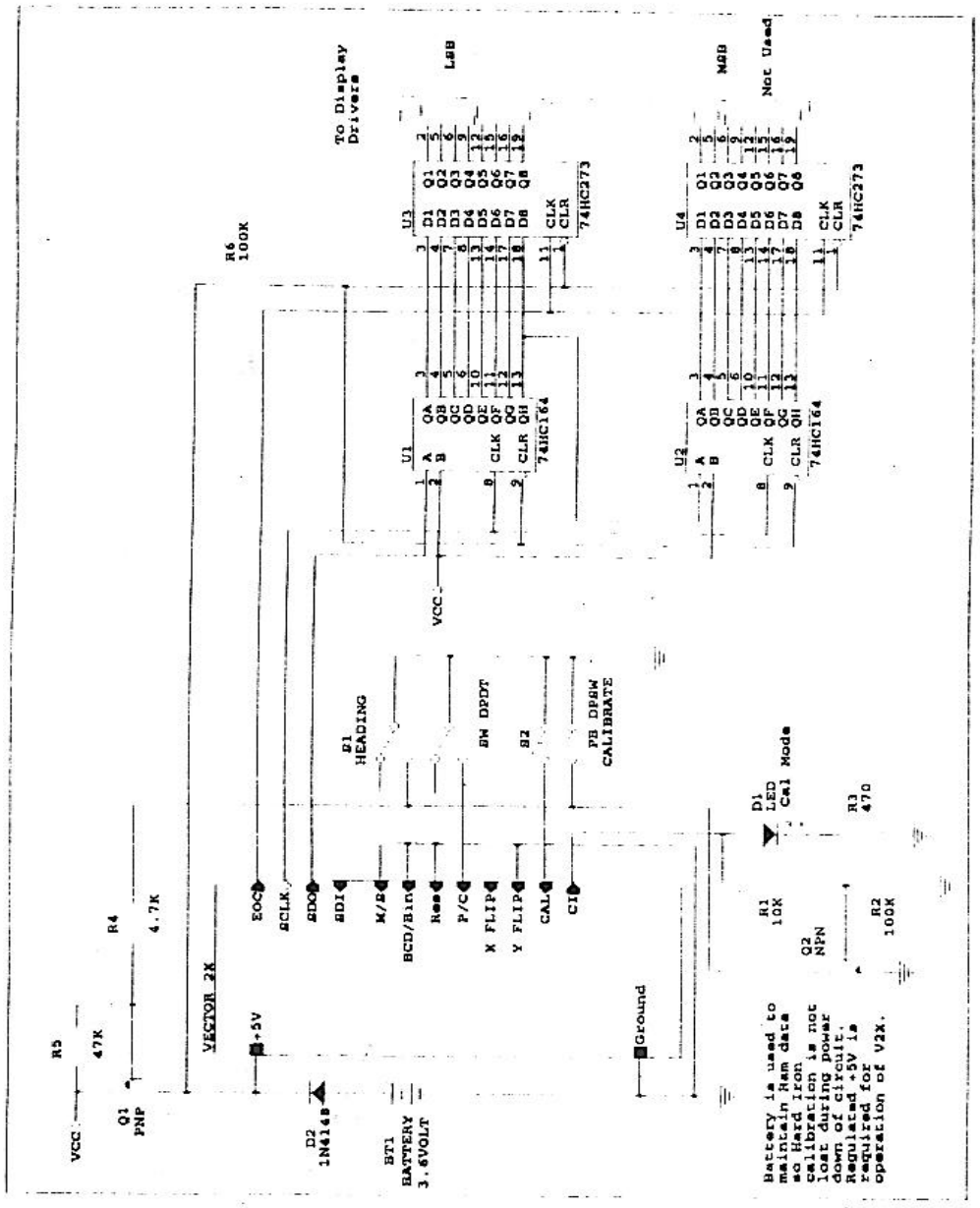

Figure A1: Schematic for Connecting Vector 2X with Serial-to-Parallel Shift Registers

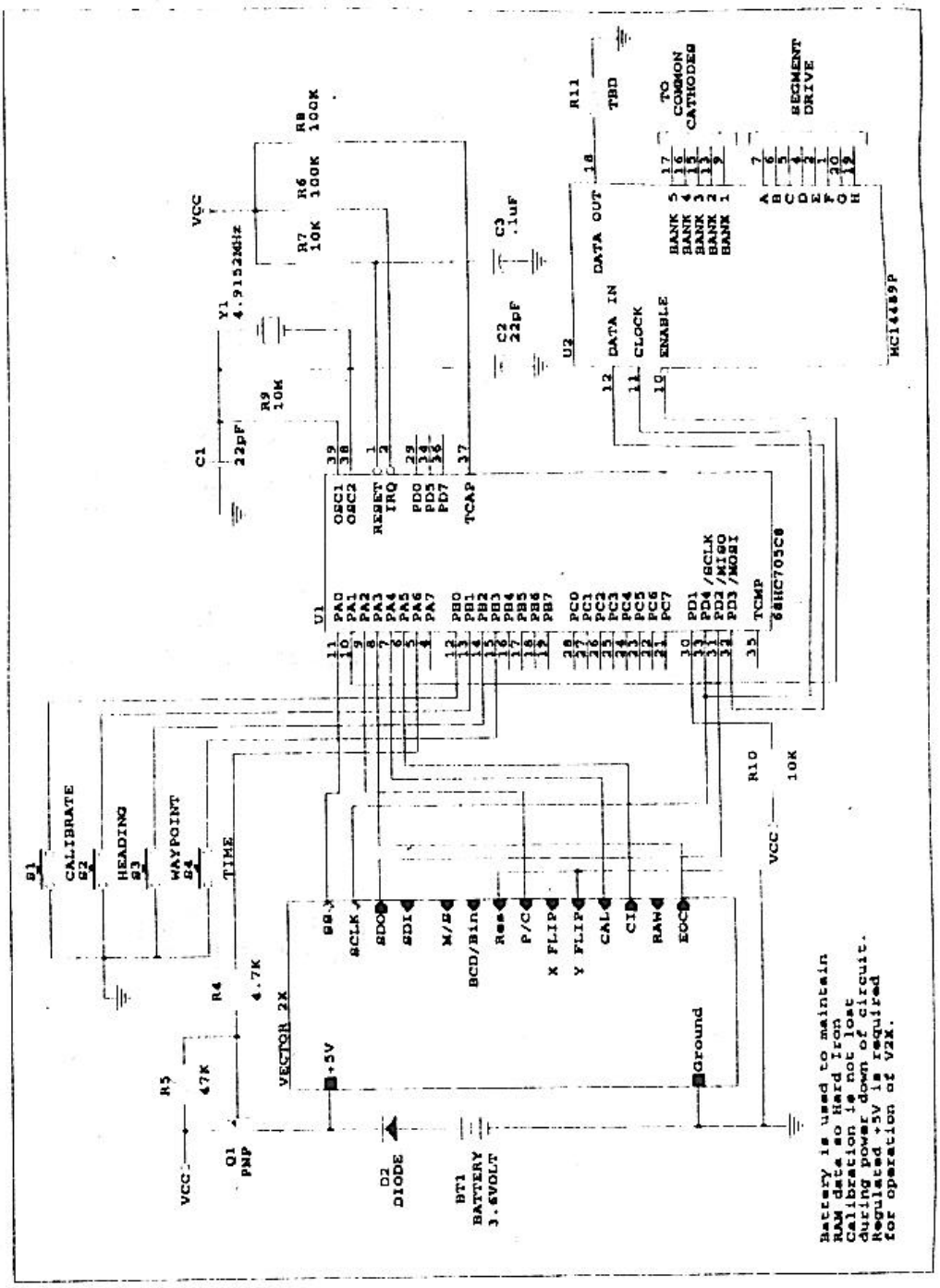

Figure A2: Schematic for Connecting Vector 2X to a Motorola Processor

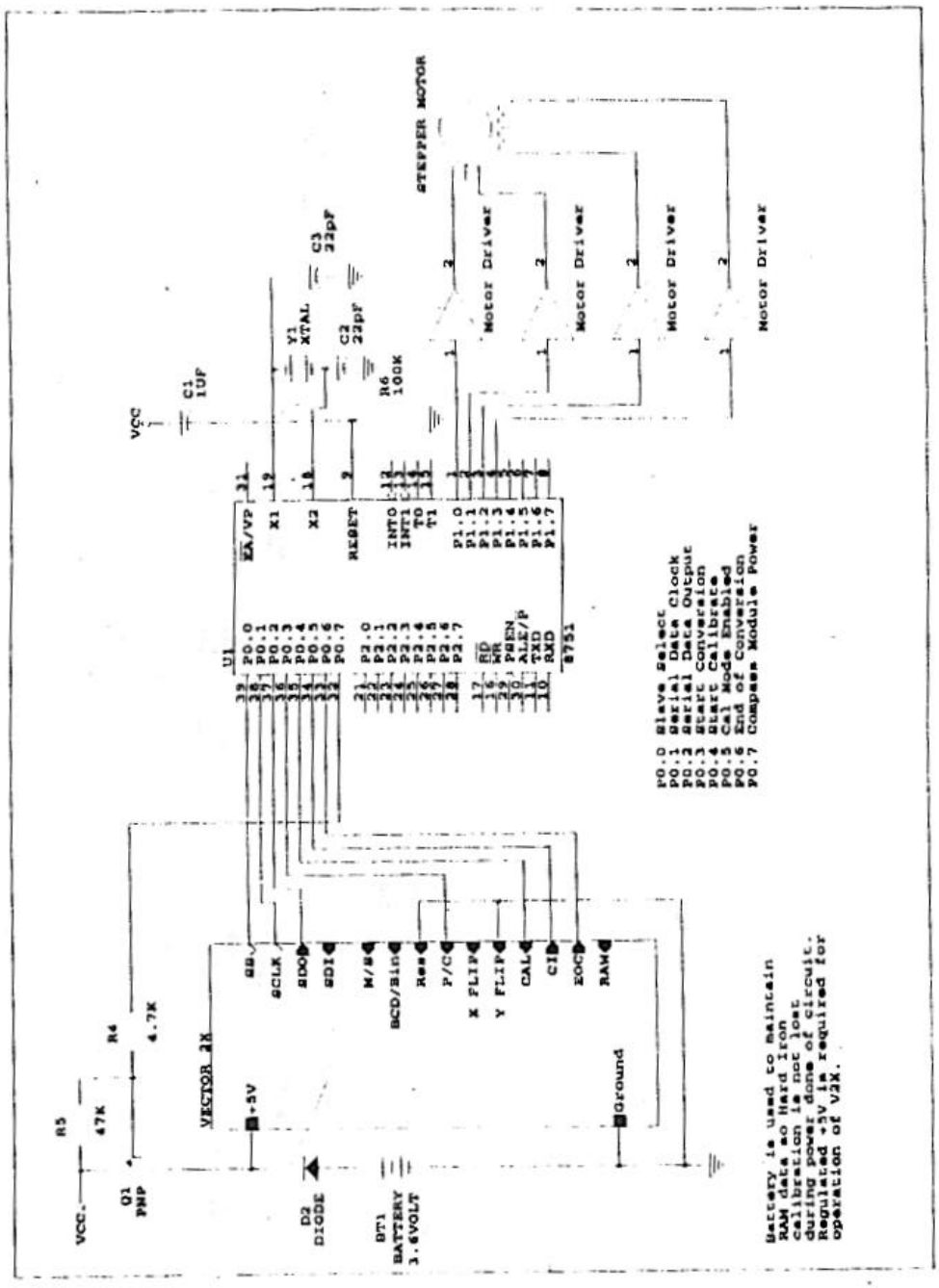

Figure A3: Schematic for Connecting Vector 2X to an Intel-Type Processor

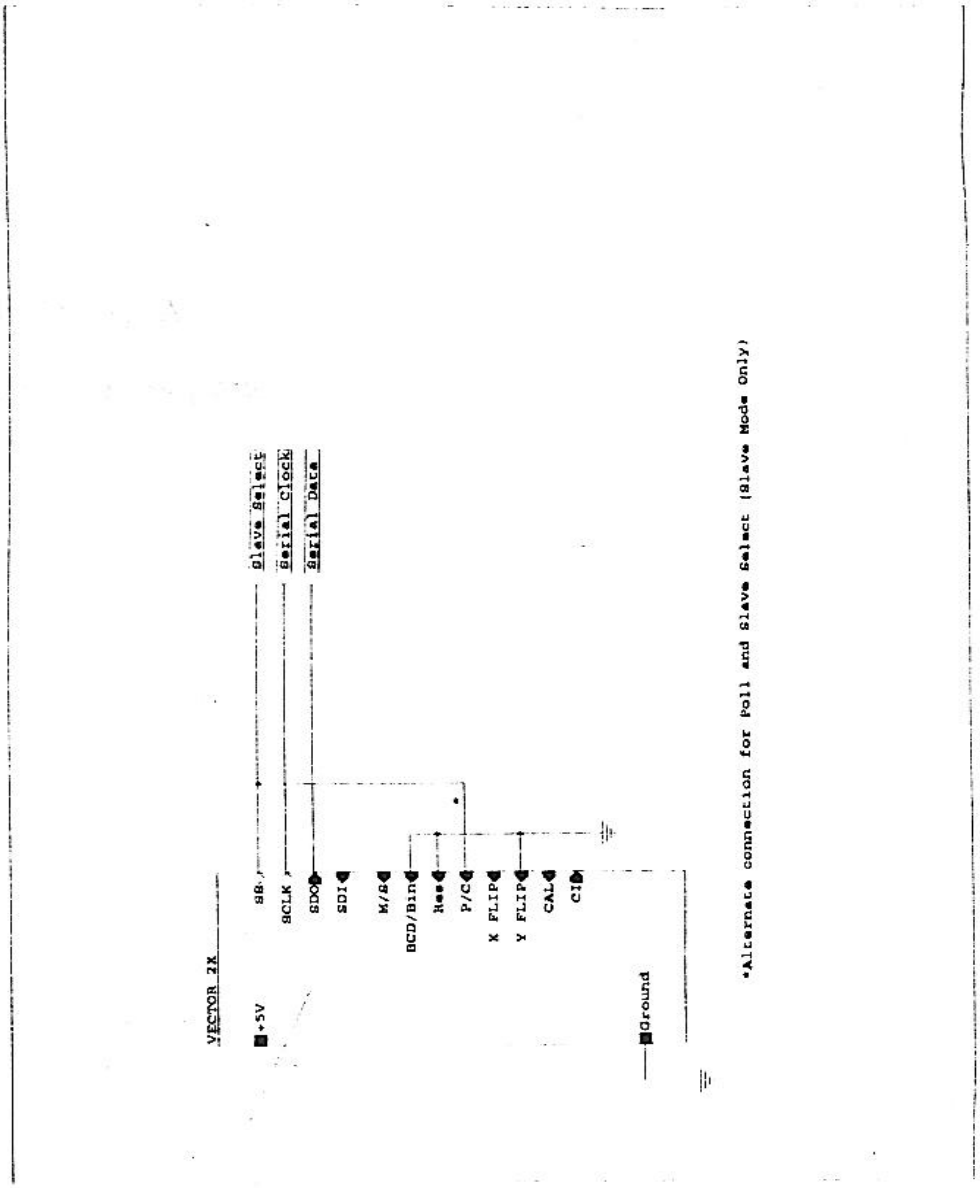

Figure A4: Schematic for Alternate Metod of Connecting Vector 2X to an Intel-Type Processor

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Appendix B

Sample SPI read Code

```
      * Sample SPI read code for Motorola 68HC705 family
      *              processor
      * Note: Not executable with schematics shown in
      *       Appendix A of V2X Application Notes!
************************************************
      *     SPI - Master mode (68HC705)
      *     Port A: Input
      *       A0:      EOC from V2X (End of Conversion)
      *       A7:      RES select (Resolution Select)
      *
      *     Port C1: Slave select bar to V2X
      *       C0:      SS (Slave Select [bar]) to V2X
      *       C7:      P/C (Poll/Continuous [bar])
************************************************
      *     Equates

         EOC          equ    0    ;EOC input to processor
         RES          equ    7    ;Resolution select
         SS           equ    0    ;Slave select from processor
         POLL         equ    1    ;Poll/Continuous control

************************************************

*RAM Location

                org $050 ;ORG RAM

BYTE1           rmb    1    ;high order byte temp storage
BYTE2           rmb    1    ;low order byte temp storage

************************************************

*ROM Location

                org $200 ;ORG ROM

*     slave_read - read the 2 bytes of data from the V2X over the SPI port
*     data is returned in bytel, byte2

************************************************
slave_read:
*Start V2X to acquire heading

      bclr poll,portc          ;drop POLL line to compass
      jsr delay10msec          ;wait a while -10 msec
      Bset poll,portc          ;raise POLL line after 10 msec
```

```
*Wait for V2X to complete conversion for heading data
      jsr   waiteoc  ;now wait for EOC to go high

*Retrieve data from V2X

        bclr 1,portc          ;lower SS line to enable xfer
        tst SPSR              ;see if SPI is clear
        sta SPDR              ;write to SPDR to start SPI xfer

*Wait for data transfer to complete
rspiflp1:
      brclr 7,spsr,rspiflp1     ;keep looping till SPI xfer
                                ;done

*Get the first data byte

lda SPDR              ;
sta BYTE1             ;put in BYTE1 reg
jsr delayinterb       ;delay between bytes
clra                  ;set a = 0

*Start transfer of second byte
    sta SPDR ;write to SPI

*Wait for data transfer to complete
rspiflp2:
      brclr 7,spsr,rspiflp2     ;keep looping till done

*Get the second data byte
      1da SPDR     ;get second byte
      sta byte2    ;

**********************************************************

*     Waiteoc: after the poll has been strobed, wait for the
      eoc to go high to mark end of measurements and computations

**********************************************************
waiteoc:

          brclr EOC,Porta,waiteEOC          ;branch if EOC bit is
                                            ;clear keep looping
                                            ;till EOC returns high
          rts
```

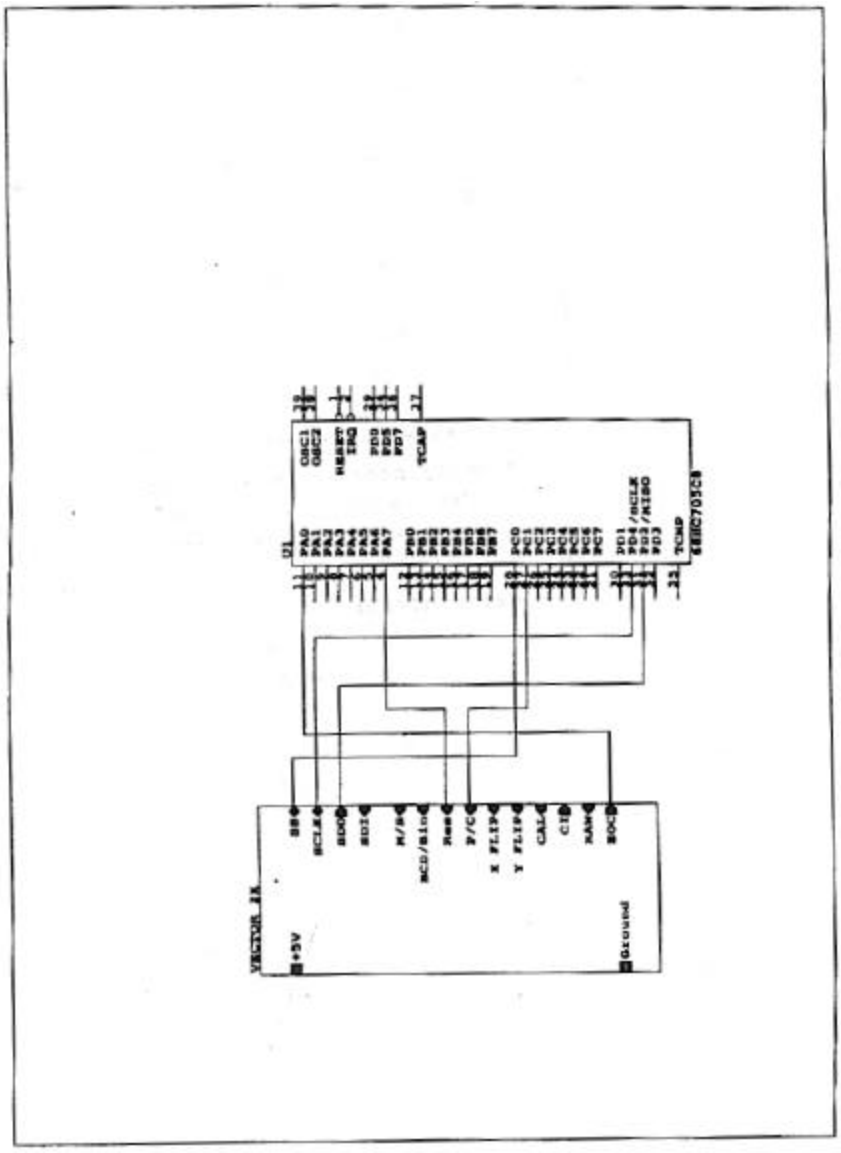

Figure B1: Schematic for SPI read Code Example

```
************************************************

* Delay 10msec - delay 10 milliseconds
* uses a & x registers for delay countdown

************************************************

delay 10msec:

        1dx     #!20    ;20 passes of olp: delay loop
        Bra     Olp
Olp:
        1da     #!156   ;156 x 3    sec delay
ilp:
        deca
        bne     ilp
        decx
        bne     olp
        rts


************************************************

* delayinterb - delay about 160    sec between bytes read in
* order to give time to SPI to elad second byte.

************************************************

delayinterb:

        1da     #!50    ;50 x 3    sec
        bra     oOlp    delay
dilp:
        deca
        bne     dilp
        rts
```